In the Claims:

1. (Currently Amended) Method of manufacturing a semiconductor device (10) in which a semiconductor body ~~(1)~~ of silicon is provided, at a surface thereof, with a first semiconductor region ~~(4)~~ of a first conductivity type, in which region a second semiconductor region ~~(2A,3A)~~ of a second conductivity type, opposite to the first conductivity type, is formed forming a pn-junction with the first semiconductor region ~~(4)~~ by the introduction of dopant atoms of the second conductivity type into the semiconductor body ~~(1)~~, and wherein, before the introduction of said dopant atoms, an amorphous region is formed in the semiconductor body ~~(1)~~ by means of an amorphizing implantation of inert atoms, and wherein, after the amorphizing implantation, temporary dopant atoms are implanted in the semiconductor body ~~(1)~~, and wherein, after introduction of the dopant atoms of the second conductivity type, the semiconductor body is annealed by subjecting it to a heat treatment, characterized in that dopant atoms of the second conductivity type are introduced into the semiconductor body ~~(1)~~ by means of ion implantation, and the semiconductor body is annealed by a heat treatment at a temperature in the range of about 500 to about 800 degrees Celsius.

2. (Currently Amended) Method according to claim 1, characterized in that the semiconductor body ~~(1)~~ is annealed by a heat treatment at a temperature in the range of 550 to about 750 degrees Celsius.

3. (Currently Amended) Method according to claim 1, characterized in that the implantation of the temporary dopant atom is performed before the implantation of the dopant atoms of the second conductivity type, and between these implantations the semiconductor body ~~(1)~~ is annealed by a further heat treatment in the same temperature range as the other heat treatment.

4. (Currently Amended) Method according to claim 1 wherein the semiconductor device is formed as a field effect transistor, in which method the semiconductor body ~~(1)~~ of silicon is provided, at the surface thereof, with a source region and a drain region ~~(2,3)~~ of the second conductivity type, which are both provided with extensions ~~(2A,3A)~~, and with

a channel region ~~(4)~~ of the first conductivity type between the source region and the drain region ~~(2,3)~~, and with a gate region ~~(5)~~ separated from the surface of the semiconductor body ~~(1)~~ by a gate dielectric ~~(6)~~ above the channel region ~~(4)~~, characterized in that first semiconductor region ~~(4)~~ is formed as a part of the channel region ~~(4)~~ and the source and drain extensions ~~(2A,3A)~~ are formed as a part of the second semiconductor region ~~(2A,3A)~~.

5. (Original) Method as claimed in claim 1, characterized in that for the first conductivity type the n-conductivity type is chosen, for the dopant atoms of the second conductivity type Boron atoms are chosen and for the temporary dopant atoms Fluor atoms are chosen.

6. (Original) Method according to claim 3, characterized in that for the amorphizing implantation of inert ions, ions are chosen from a group comprising Ge, Si, Ar or Xe.

7. (Original) Method as claimed in claim 1, characterized in that for the annealing heat treatments a time is chosen between 1 second and 10 minutes.

8. (Currently Amended) A semiconductor device ~~(10)~~ obtained with a method as claimed in claim 1.

9. (Currently Amended) A semiconductor device ~~(10)~~ as claimed in claim 8, characterized in that the device comprises a field effect transistor.

10. (New) A method according to claim 1, wherein the anneal is carried out at a temperature to mitigate the deactivation of the dopant atoms of the second conductivity type.

11. (New) A method according to claim 1, further including, after introduction of the dopant atoms of the second conductivity type, controlling the temperature of subsequent manufacturing steps for the semiconductor device to not exceed about 800 degrees Celsius.

12. (New) A method of manufacturing a semiconductor device having a silicon semiconductor body including a first semiconductor region of a first conductivity type, the method comprising:

implanting inert atoms to form an amorphous region in the first semiconductor region;

after implanting inert atoms,

implanting temporary dopant atoms at the amorphous region,

ion-implanting dopant atoms of a second conductivity type at the amorphous region, the second conductivity type being opposite the first conductivity type; and

after ion-implanting the dopant atoms of a second conductivity type, annealing the semiconductor device via heat treatment at a temperature in the range of about 550 to about 750 degrees Celsius to recover the amorphous region and to form a second semiconductor region including the dopant atoms of the second conductivity type, the first and second semiconductor regions forming a pn-junction therebetween.

13. (New) The method of claim 12, wherein the step of annealing includes annealing the semiconductor device at a temperature that mitigates deactivation of the dopant atoms of the second conductivity type.

14. (New) The method of claim 12, wherein, after the step of annealing, the temperature of subsequent manufacturing steps for the semiconductor device is controlled to not exceed about 800 degrees Celsius.

15. (New) The method of claim 12, wherein the step of implanting temporary dopant atoms is carried out before the step of ion-implanting dopant atoms of a second conductivity type.

16. (New) The method of claim 12, wherein the step of implanting temporary dopant atoms is carried out after the step of ion-implanting dopant atoms of a second conductivity type.

17. (New) The method of claim 12,

wherein the step of implanting temporary dopant atoms is carried out before the step of ion-implanting dopant atoms of a second conductivity type, and

further including, prior to ion-implanting dopant atoms of a second conductivity type, annealing the semiconductor device via heat treatment at a temperature in the range of about 500 to about 800 degrees Celsius.

18. (New) The method of claim 12, wherein the implanting steps are carried out in part of a channel region of a field-effect transistor, adjacent to an active region, to form an extension of the active region that underlies a surface of the channel region.

19. (New) The method of claim 12, wherein

the first conductivity type is the n-conductivity type;

ion-implanting dopant atoms of a second conductivity type includes ion-implanting Boron atoms; and

implanting temporary dopant atoms includes implanting Fluor atoms.

20. (New) The method of claim 12, wherein implanting inert atoms includes implanting inert atoms selected from the group of: Ge, Si, Ar or Xe.